**Date :**

**Exp No: 1**

# TWO STAGE RC COUPLED AMPLIFIER

## AIM:

To study the frequency response of a two stage RC-coupled amplifier and calculation of gain and band width.

## OBJECTIVES

1. To set up and design a two stage RC coupled amplifier for a gain of 100.
2. To study the effect of coupling capacitor
3. To calculate the Bandwidth of the designed amplifier.

**COMPONENTS REQUIRED**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S No:** | **Component** |  | **Specification** | | **Quantity** |
| 1 | Transistor | Q1,Q2 | BC547 | | 2 |
| 2 | Resistor | RE | 680Ω | 2 | |
| RS | 120 Ω | 2 | |
| R2 | 10K Ω | 2 | |
| R1 | 47K Ω | 2 | |
| RC1 | 1.8K Ω | 1 | |
| RC2 | 1.5K Ω | 1 | |
| 3 | Capacitor | CCC | 4.7μF | | 2 |
| CE | 47μF | | 2 |
| CC3 | 3.3μF | | 1 |

## THEORY

RC coupled CE amplifier is widely used in audio frequency applications in radio and TV receivers. It is usually employed for voltage amplification. Base current controls the collector current of a common emitter amplifier. A small increase in the base current results in a relatively large increase in the collector current. The emitter base junction must be forward biased and the collector base junction must be reverse biased for the proper functioning of an amplifier.

More stages of an RC coupled amplifier can be used in cascade to increase the voltage gain of an amplifier. A two stage amplifier provides an overall voltage gain of A1A2, if A1 and A2 are the gains of the first and the second stages respectively. Since each stage provides a phase inversion, the final output is in phase with the input.

The input impedance of the second stage is in parallel with Rc of the first stage. The voltage gain A1 of the first stage is

A1 = RC || Z in(second stage) / re

Where Z in (second stage) = R1 || R2 || hfe re

The voltage gain A2 of the second stage is:

A2=RC || RL / re

## CIRCUIT DETAILS:

1. A coupling capacitor Cc is used to connect the output of first stage to the base of second stage and so on. If this is not used, the bias conditions of the next stage will be drastically changed due to the shunting effect of Rc.

2. Biasing Circuits: The resistances R1, R2 and RE form the biasing and stabilization circuit. The biasing circuit must establish a proper operating point, otherwise a part of the negative half cycle of the signal maybe cutoff in the output. The maintenance of the operating point stable (independent of temperature variations or variations in transistor parameters) is known as stabilization. One of the methods of achieving operating point stability is by making use of a resistive biasing circuit.

3. Input Capacitor: An electrolytic capacitor is used to couple the signal to the base of the transistor. If it is not used, the signal source resistance will come across R2 and thus change the bias. The capacitor C1 allows only ac signal to flow but isolates the signal source from R2.

4. Emitter Bypass capacitor: An emitter bypass capacitor, CE is used in parallel with RE to provide a low reactance path to the amplified ac signal.

5. Swamping Resistor: To stabilize the voltage gain by making it independent of re' .

## OPERATION

When an ac signal is applied to the base of the first transistor, it appears in the amplified form across its collector load RC.The amplified signal developed across Rc is given to base of next stage through coupling capacitor Cc. The second stage does further amplification of the signal.

## PROCEDURE

1. Connections are made as shown in the circuit diagram.(first stage)
2. Verify the circuit
3. Set the power supply to the desired level
4. Connect the power supply to the circuit on the bread board
5. Check the DC conditions, Collector current level
6. If the DC conditions are not proper then check the design of biasing devices
7. Set the function generator to the desired amplitude level
8. A sinusoidal input of 20 mV is applied as input.
9. Connect the function generator output to the circuit on the bread board
10. Check whether desired gain is there for the first stage
11. Connect the second stage on to the bread board
12. Repeat the steps 5-10
13. The output voltage in the first stage and at the second stage is noted.
14. The output waveforms are also plotted
15. Frequency response is plotted on to the semi-log graph paper

## FREQUENCY RESPONSE

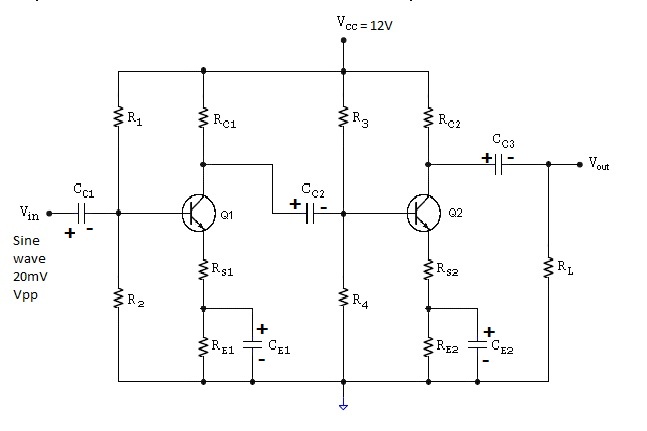
The voltage gain drops off at low (<50Hz) and high (>20 KHz) frequencies whereas it is uniform over mid-frequency range (50 Hz to 20 KHz).

1. At low frequencies, the reactance of coupling capacitor Cc is quite high and hence very small part of signal will pass one stage to the next sage. Moreover, CE cannot shunt the emitter resistance RE effectively because of its large reactance at low frequencies.
2. At high frequencies, the reactance of CC is very small and it behaves as a short circuit. This increases the loading effect of next stage and serves to reduce the voltage gain. Moreover at high frequency, capacitive reactance of base-emitter junction is low which increase the base current. This reduces the gain.
3. At mid frequencies, the voltage gain is constant. The effect of coupling capacitors in this frequency range is such as to maintain a uniform voltage gain

## BC547 PIN CONFIGURATION



## CIRCUIT DIAGRAM: -

****

## DESIGN:-

Let VCC = 12V, IC = 2 mA , β = 125, AV = 100

Choose BC547 transistor.

Voltage gain AV  = 100 = A1 X A2

AV1 =AV2 = 10

**To select RE1 and RE2**

VRE = 10% of Vcc = 1.2V

RE = VRE = 1.2 = 600Ω

IE 2 x 10-3

Choose RE = RE1=RE2 = 680 Ω.

**To select RS1 and RS2**

re = 25mV = 25 x 10-3 = 12.5

IE 2 x 10-3

RS = 10re = 10 x 12.5 = 125 Ω.

Choose RS = RS1=RS2 = 120 Ω.

RS1 is not bypassed by CE1. So RS1 provides series feedback. For firm voltage divider bias with less value of R2, Q-point will be more stable with input impedance less.

**To select R2 and R4**

LetR2 ≤ 0.1 × β × (RS + RE)

R2 ≤ 0.1 x 125 (120 + 680)

Choose R2 =R4= 10K.

**To select R1 and R3**

VR2 = VBE + VRS1 + VRE1

VR2= 0.6 + (2 x 10-3 x 120) + 1.2 = 2.04V

VR1 = VCC - VR2 = 12 – 2.04 = 9.96V

R1 =

R1 = = 48.82K

Choose R1 =R3 = 47K.

**To select CC1 and CC2**

Input impedance = R1 || R2|| β (RS1 + re)

Zin1 =

Zin1 =

Zin1 = 5.5K

Let XCC ≤ 10% of input impedance

XCC< 10% of Zin =10% of 5.5K = 550 Ω

At f =50Hz, CCC =

CCC = = 5.78µF

Select CCC = CC1 = CC2= 4.7µF

**To select CE1 and CE2**

Let XCE1< 10% of RE1 = 68Ω

At f = 50Hz, CE =

CE = = 46.8µF

Select CE = CE1= CE2 = 47µF.

**Select R1 = R3 = 47k, R2 = R4 = 10K, RE1 = RE2 = 680 Ω, RS1 =RS2 =120 Ω,**

**CC1 = CC2= 4.7µF, CE1 =CE2 = 47µF.**

**To select RC1**

Input impedance = Zin = R1 || R2|| β (RS1 + re)

Zin1 = Zin2 = 5.5K

A1 =

RC1 || Zin2 = A1 × (re + RS1)

A1× (re + RS1)

10× (12.5 + 120)

RC1 = 1.75K

Select RC1­ = 1.8K.

**To select RC2**

Let RL = 10k

A2 =

A2 × (re + RS2)

10 × (12.5+120)

RC2 = 1.53k

Select RC2 = 1.5K.

**To select CC3**

XCC3≤ 10% of RL = 1k

At f = 50Hz, CC3 =

CC3 =

## OBSERVATIONS:

**D.C. Conditions :( To be filled in by the student)**

|  |  |  |  |
| --- | --- | --- | --- |
| **First stage** | | **Second stage** | |
| **VRC1** |  | **VRC2** |  |
| **VRE1** |  | **VRE2** |  |
| **VRS1** |  | **VRS2** |  |
| **VCE1** |  | **VCE2** |  |
| **VR1** |  | **VR3** |  |
| **VR2** |  | **VR4** |  |
| **VBE1** |  | **VBE2** |  |

**To check DC condition**

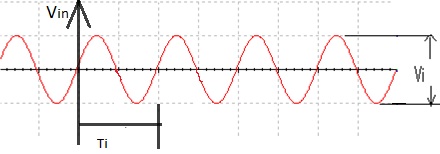
|  |
| --- |
| VCEQ1  = VCC - ICQ (RE1 + RS1 + RC1)  = 12 – 2x103 (680 +120+ 1.8x103)  = 6.8V  VCEQ2= VCC - ICQ (RE2 + RS2 + RC2)  = 12 – 2x103(680 + 120 + 1.5x103)  = 7.4V |

**Tabular Column : Vi = ……..**

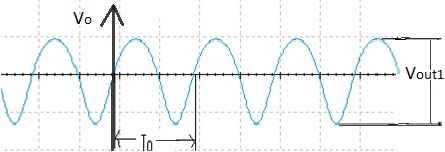
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Sl.No | Frequency | Vopp (V) | Gain, A=Vo/Vi | 20 log A |
|  |  |  |  |  |

## EXPECTED WAVEFORMS:

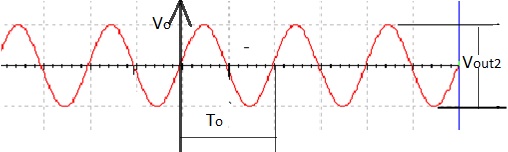
INPUT WAVEFORM:

****

FIRST STAGE OUTPUT:

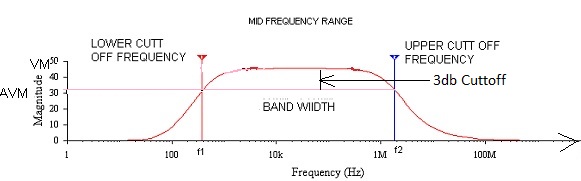
****

SECOND STAGE OUTPUT:

****

**Vout2 >Vout1>Vin**

## FREQUENCY RESPONSE:

****

## RESULT:

## INFERENCE